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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/801,564	SAULSBURY ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/27/04; 03/03/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-13 and 15-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-13 and 15-24* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendments, filed 03/03/2004 and 09/27/2004.

2. Claims 1-2, 4-13, and 15-24 are pending in the application. Claims 1, 9, and 18 are independent claims. In Amendment, claims 1, 4-6, 8-9, and 17-18 are amended, claims 3 and 14 are cancelled, and claims 23-24 are added. This action is made final.

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Objections

2. Claims 12 and 23 are objected to because of the following informalities:

Re claim 12, the applicant is advised to change the phrase "the second operand" in line 3 as "the third operand" for précised claim.

Re claim 23, the applicant is advised to write the acronym "VLIW" in full as "very long instruction word (VLIW)" for clarification.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-7, 9-13, 15-16, and 18-22 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Intel Inc. ("8XC251SB Embedded Microcontroller User's Manual").

Re claim 1, Lin et al. disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a processing core (Figure 1) comprising: a first source register (SRC1 in Figure 6) including a plurality of first operands (Figure 7a wherein each SRC1 is subdividing into plurality of operands e.g. $Source1_{7-0}$; $Source1_{15-8}$); a plurality of second operands (SRC2 in Figure 6), wherein: the plurality of second operands are equal in value to an immediate value (throughout the specification, all the elements/operands in SRC2 can set to be equal in a value), and a bit-wise inverter coupled to at least one of the first plurality of operands and the second plurality of operands (1603 in Figure 16 for subtracting operation); a destination register including a plurality of results (Figure 9 e.g. 910a-910c); a plurality of arithmetic processors (e.g. 907a-907h in Figure 9) respectively coupled to the first operands (e.g. Source1 with 906a label), second operands (e.g. Source2 with 905a) and results (e.g. 910a in Figure 9), wherein each arithmetic processor computes one of a sum (e.g. Adder label 908a in Figure 9) and a difference (e.g. Subtractor label 908a in Figure 9) of the first operand and a respective second operand (either addition or subtraction in Figure 9). Lin et al. do not disclose the immediate value is specified in an instruction that identifies the first source register. However, Intel Inc. discloses in page A-14 an add and/or subtract instruction which specifying an immediate value (e.g. #data in line 4 of ADD

instruction) and first source register (e.g. A in line 4 of ADD instruction). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add/specify the intermediate value in the instruction as seen in Intel Inc.'s invention into Lin et al.'s invention because it would enable to reduce the instruction call which leads to improve overall system performance.

Re claim 2, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 comprising an integrated circuit (Figure 1) which includes the first source register (e.g. SRC1 in 702 of Figure 7a), destination register (e.g. DEST in 706 of Figure 7a) and arithmetic processor (e.g. 109 in Figure 1 and particular function as seen in Figure 7a part 705a and 705b).

Re claim 4, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 each arithmetic processor (e.g. 109 in Figure 1) computes at least one of: the result of the first operand plus another operand plus the intermediate value (1706 in Figure 17 wherein the first operand is the first packed data; the another operand is the carry-in; and the immediate value third packed data); and the result of the first operand minus another operand minus the intermediate value.

Re claim 5, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 the immediate value is signed (e.g. format in Figure 5b and required either one/two complement for operation as seen in Figure 17 step 1703).

Re claim 6, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a prescaler which scales the immediate value (e.g. 703 in Figure 7a with saturation applied).

Re claim 7, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a first width of the first source register is a positive integer multiple of a second width of the first operand (abstract lines 5-6 and Figure 5b).

Re claim 9, Lin et al. disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 a method for performing arithmetic processing (abstract), the method comprising the steps of: loading a first and second operands from a primary source register (e.g. 702 in Figure 7a as SRC1 including a plurality sub-operands); loading a third and fourth operands (e.g. 702 in Figure 7a as SRC2 including a plurality sub-operands), wherein: the third and fourth operands are equal in value (throughout the specification, all the elements/operands in SRC2 can set to be equal in a value), scaling the third and fourth operands according to a predetermined scaling factor (e.g. 703 in Figure 7a with saturation applied); performing an arithmetic function (e.g. Adder/subtractor operation in 907a in Figure 9) on the first and third operands to produce a first result (e.g. in Figure 7a $Source1_{7-0}$ as first operand and $Source2_{7-0}$ as third operands); performing the arithmetic function (e.g. Adder/subtractor operation in 907a in Figure 9) on the second and fourth operands to produce a second result (e.g. in Figure 7a $Source1_{15-8}$ as second operand and $Source2_{15-8}$ as fourth operands); and storing (e.g. 910a in Figure 9) the first and second results in a destination register (Figure 9). Lin et al. do not disclose the third and fourth operands are an immediate value specified in an instruction. However, Intel Inc. discloses in page A-14 an add and/or subtract instruction which specifying an immediate value (e.g. #data in line 4 of ADD instruction) and first source register (e.g. A in line 4 of ADD instruction). Therefore, it would have been obvious to a person having ordinary skill in the art at the

time the invention is made to add/specify the intermediate value in the instruction as seen in Intel Inc.'s invention into Lin et al.'s invention because it would enable to reduce the instruction call which leads to improve overall system performance.

Re claim 10, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 comprising a step of inverting the third and fourth operands (714a and 714b in Figure 7b and 1603 in Figure 16 for subtracting operation).

Re claim 11, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 further comprising a step of adjusting at least one of the first and second results to avoid saturation of the destination register (703 in Figure 7a as saturation applied).

Re claim 12, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 wherein the step of performing an arithmetic function (e.g. addition in Figure 9) on the first and third operands comprises calculating the first operand plus the second operand plus a positive integer (1706 in Figure 17 wherein the first operand is the first packed data; the positive integer is the carry-in; and the second operand is third packed data).

Re claim 13, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 wherein the step of performing an arithmetic function (e.g. subtraction in Figure 9) on the second and fourth operands comprises calculating the second operand minus the fourth operand minus a positive integer (1706 in Figure 17 wherein the first operand is the first packed data; the positive integer is the carry-in; and the second operand is third packed data).

Re claim 15, Lin et al. further disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 wherein the predetermined scaling factor is divisible by two (col. 9 lines 1-8).

Re claim 16, Lin et al. further disclose in Figures 1, 4a, 6-9, 12, and 16-17 wherein the two performing steps (e.g. 801a and 801b in Figure 8) are performed, at least partially, coextensive in time (Figures 8-9).

Re claim 18, it has same limitations as cited in claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claims 19-20, Lin et al. do not disclose the immediate value has a width of nine or thirteen bits. However, it is obvious to application choice to have the immediate value has a width of nine or thirteen bits. Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to have the width of the immediate value of nine or thirteen bits in Lin et al.'s invention because it would enable to reduce the system circuitry for that particular application needs.

Re claim 21, it has same limitations as cited in claim 16. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 16.

Re claim 22, it has same limitations as cited in claim 11. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

5. Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Intel Inc. ("8XC251SB Embedded Microcontroller User's Manual"), as applied to claims 1 and 9 above, and further in view of Beck et al. (U.S. 3,993,891).

Re claim 8, Lin et al. in view of Intel Inc. disclose in Figures 1, 4a, 6-7, 9, 12, and 16-17 the sum and the difference are perform on the same adder (e.g. 907a in Figure 9).

Lin et al. in view of Intel Inc. do not disclose the adder is carry look-ahead. However, Beck et al. disclose in Figure 6 a carry look-ahead adder is used to perform add/subtract (col. 8 lines 55-65). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to use the carry look-ahead adder as seen in Beck et al.'s invention into Lin et al. in view of Intel Inc.'s invention because it would enable to increase the large system performance (abstract).

Re claim 17, it is a method claim of claim 8. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

6. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being obvious over Lin et al. (U.S. 5,959,874) in view of Intel Inc. ("8XC251SB Embedded Microcontroller User's Manual"), as applied to claims 1 and 9 above, and further in view of Slavenburg et al. (U.S. 6,141,675).

Re claim 23, Lin et al. in view of Intel Inc. do not disclose the instruction is a VLIW instruction. However, Slavenburg et al. disclose in Figure 1 the instruction is a VLIW instruction (col. 4 lines 9-15). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a VLIW instruction as seen in Slavenburg et al.'s invention into Lin et al. in view of Intel Inc.'s invention because it would enable to speed up the process and reduce complexity by execute simultaneous operation using a single instruction (col. 4 lines 9-15).

Re claim 24, Lin et al. in view of Intel Inc. do not disclose the steps of the method are initiated by a single instruction issue. However, Slavenburg et al. disclose in Figure 1 the process is initiated by a VLIW instruction (col. 4 lines 9-15). Therefore, it would

have been obvious to a person having ordinary skill in the art at the time the invention is made to initiate by a VLIW instruction as seen in Slavenburg et al.'s invention into Lin et al. in view of Intel Inc.'s invention because it would enable to speed up the process and reduce complexity by execute simultaneous operation using a single instruction (col. 4 lines 9-15).

Response to Arguments

7. Applicant's arguments with respect to claims 1-2, 4-13, and 15-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

November 2, 2004

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